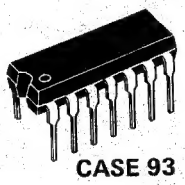
MOS

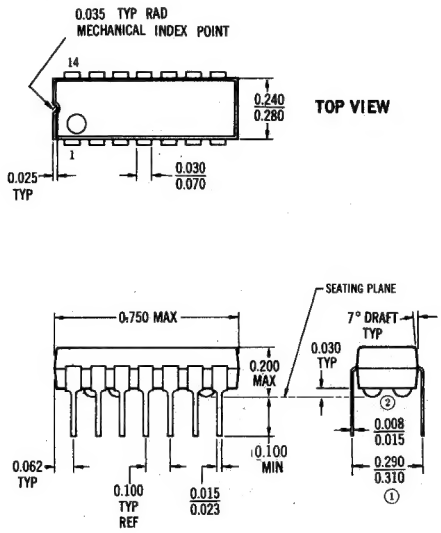
INTEGRATED CIRCUITS

MC1120P SERIES

This low-cost MOS integrated circuit series is designed specifically for electronic organ applications.



CASE 93
(TO-116)



FUNCTIONS AND CHARACTERISTICS ($V_S = -10$ V, $T_A = 25°C$)

FUNCTION	TYPE CASE 93 0 to +75°C	Output Loading Factor Each Output	Output Voltage Swing Volts	Operating Frequency kHz	Total Power Dissipation mW typ/pkg
Dual Keyer Gate with Snub Inputs	MC1120	5	12	0 to 100	10
Frequency Divider (Four Stage)	MC1124	5	10	0 to 100	190

MAXIMUM RATINGS

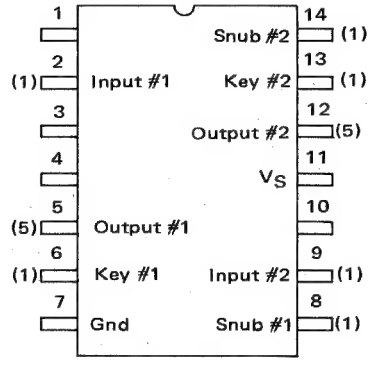
RATING	VALUE	UNIT
Power Supply Voltage	−40 to +0.3	Vdc
Input Voltage — MC1120P MC1124P	−40 to +0.3 −30 to +0.3	Vdc
Operating Temperature Range	0 to +75	°C
Storage Temperature Range	−55 to +125	°C

DUAL KEYER GATE
With Snub Inputs

MC1120P

A monolithic circuit consisting of two gates with key and snub inputs.

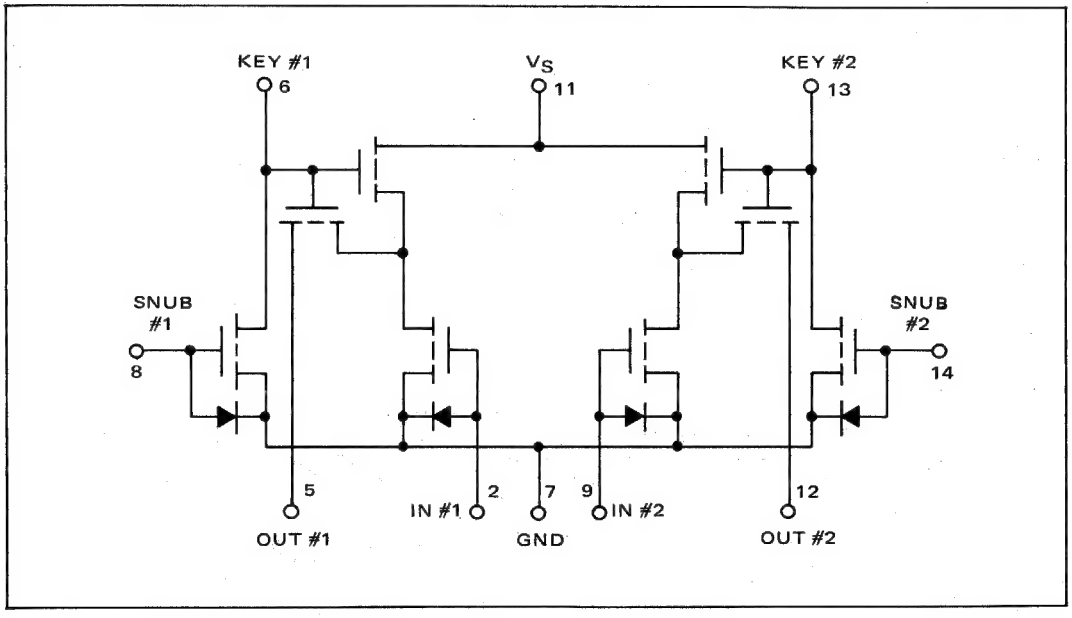
- Noise Immunity = 1.0 Volt
- Minimum Fan-Out = 5
- Temperature Range = 0 to +75°C



Number in parenthesis = loading factor

CASE 93
(TO-116)

CIRCUIT SCHEMATIC



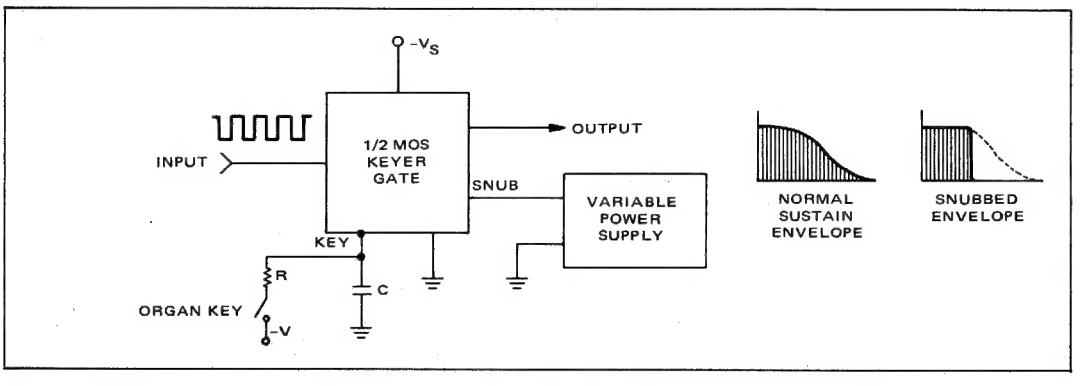
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Source Voltage	V_S	-40 to +0.3	Vdc
Input, Snub, Key Voltages	V_{in}, V_{SN}, V_K	-40 to +0.3	Vdc
Operating Temperature Range	T_A	0 to +75	°C
Storage Temperature Range	T_{stg}	-55 to +125	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Pin Under Test	Min	Max	Unit	Test Conditions Vdc ± 1%					Ground
						V_{IL} -2.5	V_{IH} -15	V_K -20	V_{max} -40	V_S -10	
						Applied to pins listed below:					
Source Supply Drain Current	I_S	11	-	1.0	mAdc	-	9,2	6,13	-	11	7,8,14
Input Current	I_{in}	2	-	100	μAdc	-	-	-	2	-	6,7
		9	-	100	μAdc	-	-	-	9	-	7,13
Snub Current	I_{SN}	8	-	100	μAdc	-	-	-	8	-	6,7
		14	-	100	μAdc	-	-	-	14	-	7,13
Key Current	I_K	6	-	100	μAdc	-	-	-	6	-	2,7,8
		13	-	100	μAdc	-	-	-	13	-	7,9,14
Key Current (Snub On)	$I_{K(on)}$	6	70	-	μAdc	-	8	6	-	-	2,7
		13	70	-	μAdc	-	14	13	-	-	7,9
Key Current (Snub Off)	$I_{K(off)}$	6	-	1.0	μAdc	8	-	6	-	-	2,7
		13	-	1.0	μAdc	14	-	13	-	-	7,9
Logical "1" Output Voltage	V_{OL}	5	-	-2.0	Vdc	-	-	2,6	-	11	7
		12	-	-2.0	Vdc	-	-	9,13	-	11	7
Logical "0" Output Voltage	V_{OH}	5	-9.0	-	Vdc	-	-	6	-	11	2,7
		12	-9.0	-	Vdc	-	-	13	-	11	7,9

TYPICAL APPLICATION

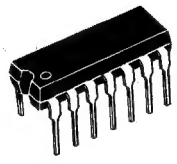


Closing of the organ key "enables" the KEYER GATE, permitting subsequent pulses applied to the signal input to pass through the gate, and simultaneously charges capacitor C. When the key is released the stored charge maintains the gate conduction until charge is removed. The SNUB line provides a means of varying the total resistance in parallel with the capacitor by controlling the series impedance of the MOS transistor. Therefore the length of time that the note is sustained after the key is released depends upon the snub voltage.

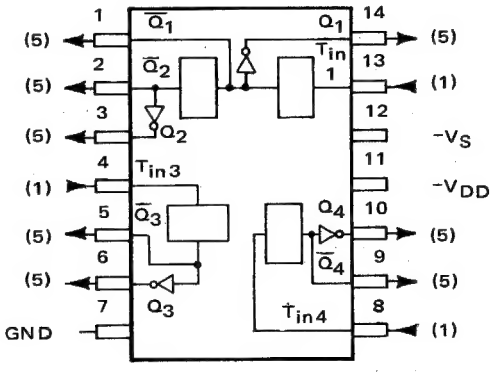
MC1124P

A monolithic circuit consisting of four flip-flops with single rail inputs and Q and $\overline{Q}$ outputs.

- Toggle Frequency = DC to 500 kHz
- Noise Immunity = 1.0 Volt
- Minimum Fan-Out = 5
- Temperature Range = 0 to +75°C



CASE 93
(TO-116)

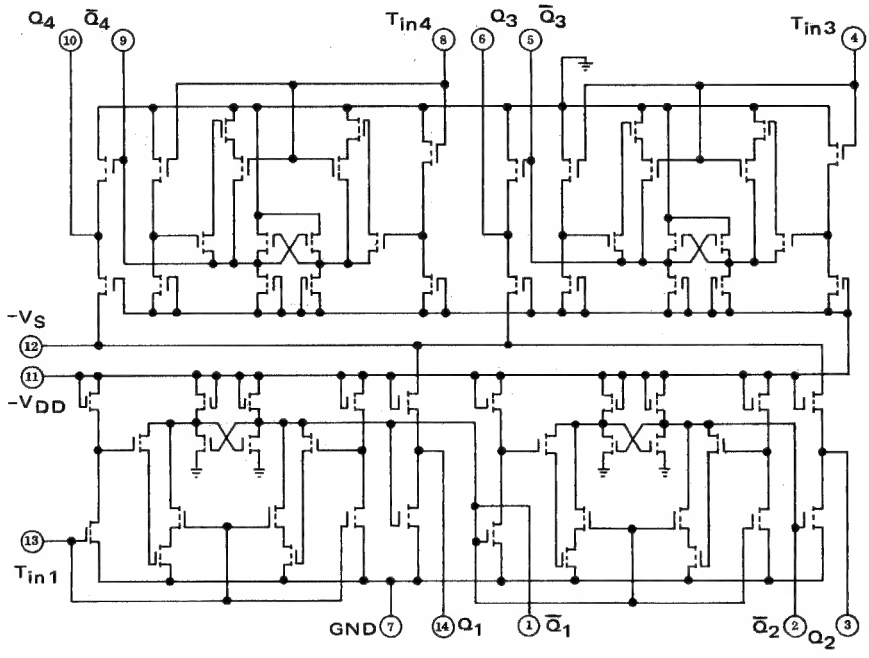


Number in parenthesis = loading factor

NOTE:

To cascade flip-flop stages, connect $\overline{Q}$ (trigger out) to T_{in} (trigger in) of the next stage.

CIRCUIT SCHEMATIC



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain Voltage	V_{DD}	-40 to +0.3	Vdc
Trigger Input Voltage	V_{in}	-30 to +0.3	Vdc
Operating Temperature Range	T_A	0 to +75	°C
Storage Temperature Range	T_{stg}	-55 to +125	°C

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	Min	Max	Unit	Test Voltages @ T_A = 25°C			Ground
						VT_{in} *	V_{DD} -30 ± 1 Vdc	V_S -10 ±0.5 Vdc	
						Applied to pins listed below:			
Drain Supply Drain Current	I_{DD}	11	-	2.5	mAdc	-	11	12	1,4,7,8,13
Source Supply Drain Current	I_{DS}	12	-	17	mAdc	-	1,2,5,9,11	12	4,7,8,13
Source Supply Leakage Current	I_{SS}	12	-	5.0	μAdc	-	-	12	1,2,3,4,5 6,7,8,9,10 11, 13, 14
"Q" Logical "0" Output Voltage	V_{OH}	3	-9.0	-	Vdc	1	11	12	7
		6	-9.0	-		4	11	12	7
		10	-9.0	-		8	11	12	7
		14	-9.0	-		13	11	12	7
"Q" Logical "1" Output Voltage	V_{OL}	3	-	-2.5	Vdc	1	11	12	7
		6	-	-2.5		4	11	12	7
		10	-	-2.5		8	11	12	7
		14	-	-2.5		13	11	12	7
"$\overline{Q}$" Logical "0" Output Voltage	V_{OH}	1	-10	-	Vdc	13	11	12	7
		2	-10	-		1	11	12	7
		5	-10	-		4	11	12	7
		9	-10	-		8	11	12	7
"$\overline{Q}$" Logical "1" Output Voltage	V_{OL}	1	-	-2.5	Vdc	13	11	12	7
		2	-	-2.5		1	11	12	7
		5	-	-2.5		4	11	12	7
		9	-	-2.5		8	11	12	7
Toggle Frequency	f_{Tog}		100	-	kHz		See Test Diagram		

*VT_{in} — Preset to desired output level by applying -20 Vdc to input then open.

TOGGLE FREQUENCY TEST DIAGRAMS AND WAVEFORMS